# **Adding PMOD IP Core block in Vivado**

# **Zynq design**

Prepared by

**Binit Kumar Pandit**

# Introduction

In this lab we have added PMOD\_ACL to the block design and seen the output of the x, y & z axis value in the terminal.

# Create a Vivado Project

1. Open Vivado by selecting **Start > All Programs > Xilinx Design Tools > Vivado 2015.4 > Vivado 2015.4.**
2. Click **Create New Project** to start the wizard. We will see the Create a New Vivado Project dialog box. Click **Next**.
3. Enter **Project name** and **Project location**. Click **Next**.
4. In the Project Type form select **RTL Project**, and click **Next**.
5. Click Boards. Search for **Zedboard Zynq Evaluation and Development Kit** and Select it. Click Next. Click **Finish.**

# Add the Digilent Library Repository

1. Find the latest release of Digilent's vivado-library repository where the version number matches the version of Vivado being used from the link <https://github.com/Digilent/vivado-library/releases>. Download the vivado-library-<version>.zip file (NOT one of the source code archives!), then extract this archive in a memorable location. This GitHub repository contains a large number of IP cores intended for use with Digilent boards, including all of Digilent's Pmod IP cores and Pmod interface description.
2. Click **Project Settings** under Project Manager.

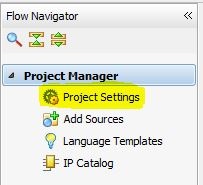


Figure 1: Project Settings to Manage IP

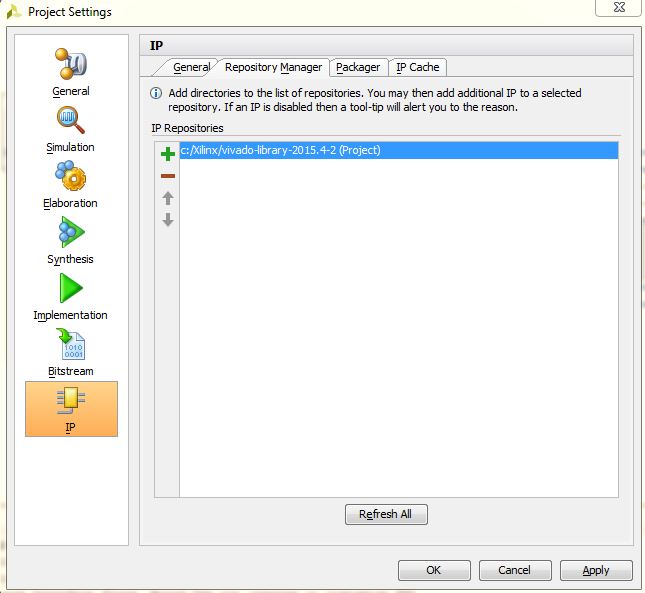
1. Click **IP** then open the **Repository Manager** tab. Click the [https://reference.digilentinc.com/_media/genesys2/plus.jpg](https://reference.digilentinc.com/_media/genesys2/plus.jpg) **Add** button and select the **vivado-library** folder from where the ZIP archive was extracted to. Click **OK**.

Figure 2: IP Repository Manager

# Add the Pmod to block design

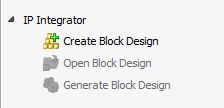
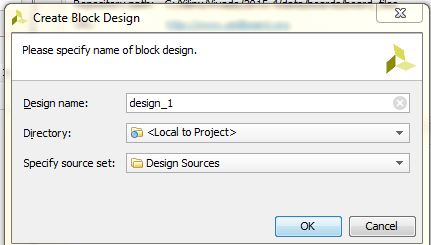
1. In the **IP Integrator**, Click on “**Create Block Design**”.

Figure 3: Creation of block design

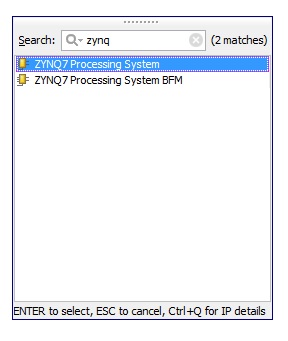
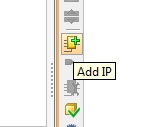
1. Click the “**Add IP**” icon. Find the “**zynq7 processing system**” IP and **double click** it.

Figure 4: Adding “**zynq7 processing system”** IP

1. Find the “**PmodACL\_v1\_0**” IP and **double click** it.

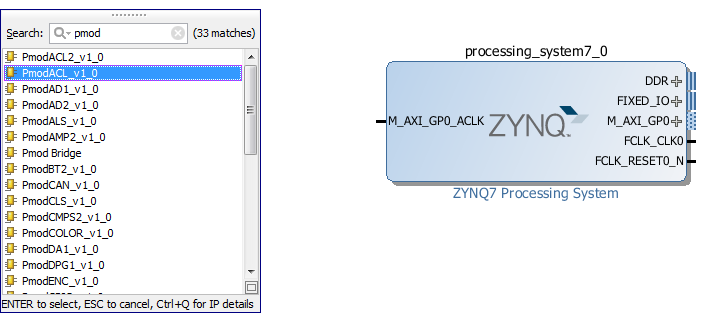


Figure 5: Addition of IP

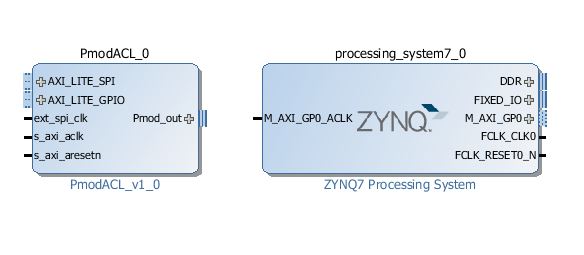
1. The block should appear in the block diagram and we should see the message “**Designer Assistance available**: **Run Block Automation** & **Run Connection Automation**”. Click the **Run Connection Automation**.

Figure 6: Addition of PmodACL\_v1\_0and zynq7 processing system

1. First, Click on **Run Connection Automation,** check all the boxes and then **OK**.

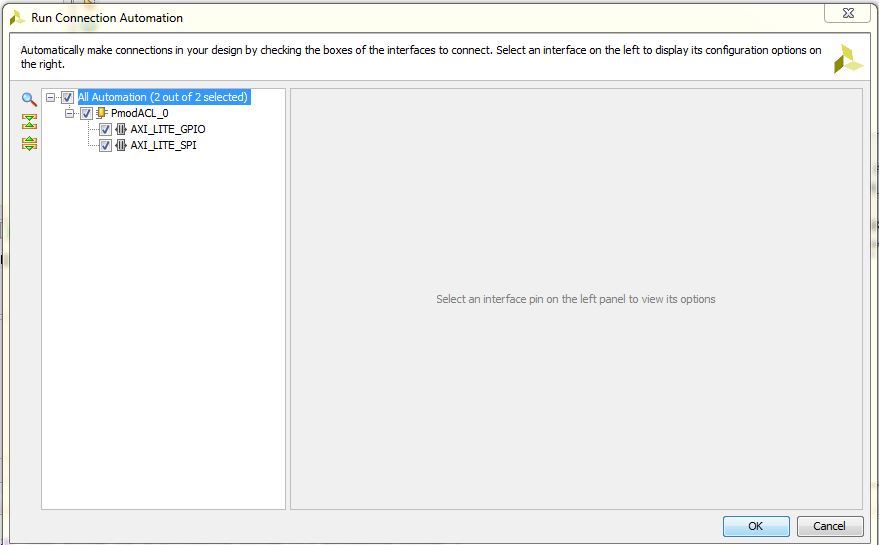


Figure 7: Connection Automation

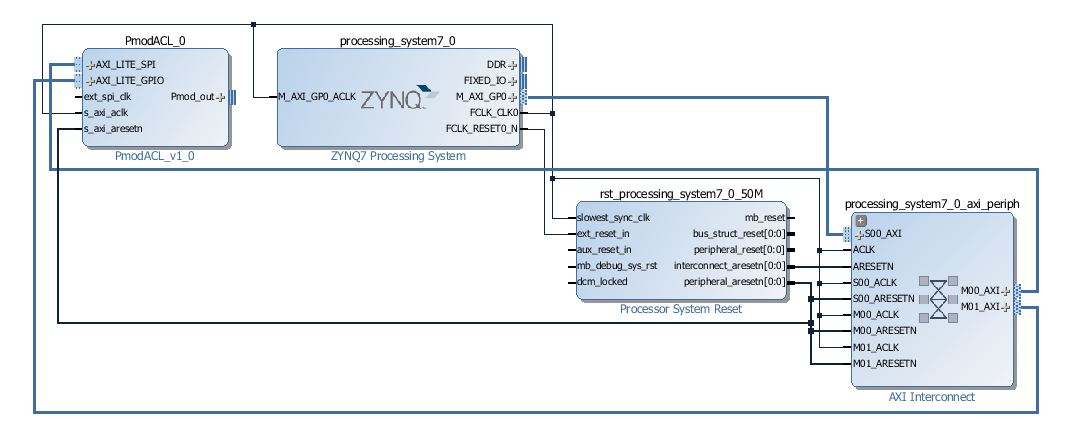
 We will be able to see this connection

Figure 8: Connection between the different IPs.

1. Then, **Run Block Automation** and click **OK**.

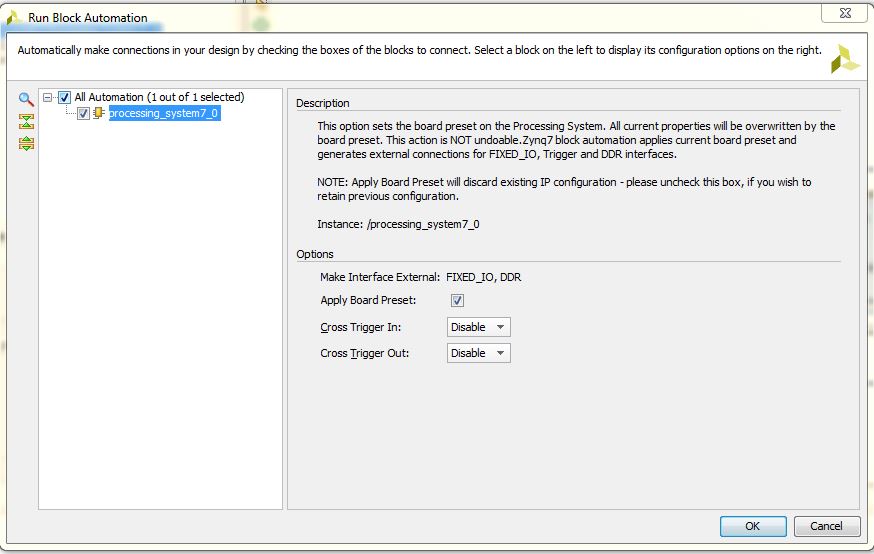


Figure 9: Block Automation

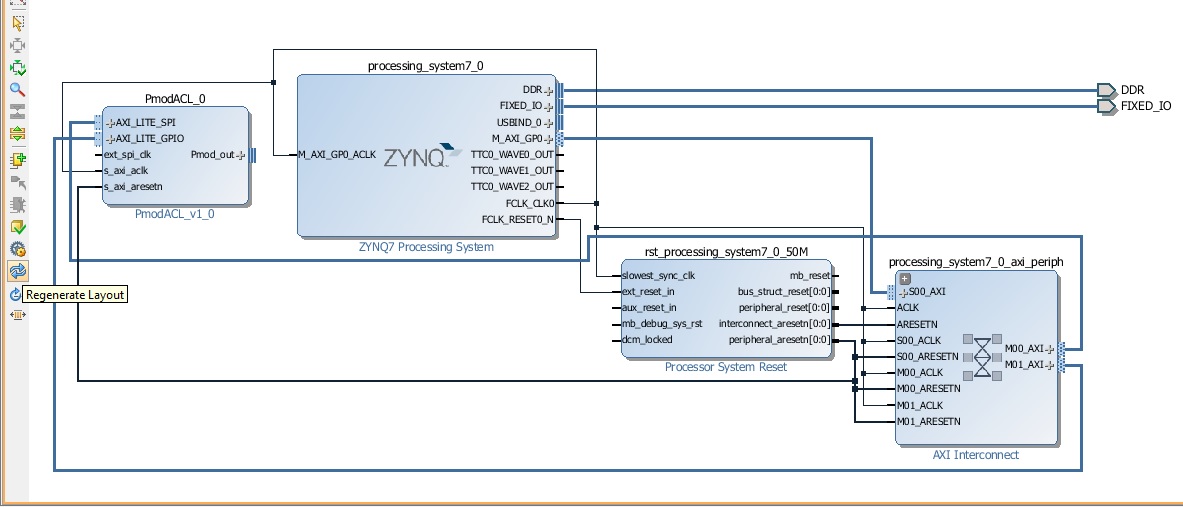


Figure 10: Overall Connection

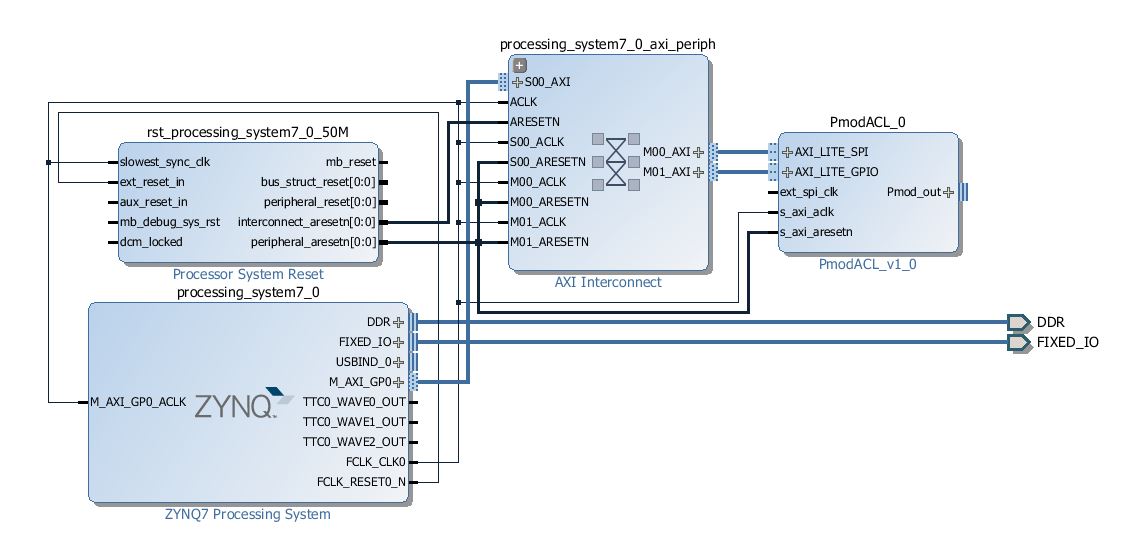
1. Regenerate Layout: Click the https://reference.digilentinc.com/_media/genesys2/regenerate.jpg **Regenerate Layout** button to rearrange our block design.

Figure 11: Regenerated layout

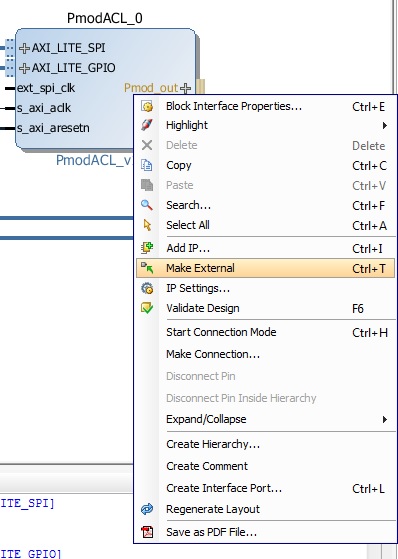
1. Right Click by selecting Pmod\_Out in the Pmod\_ACL IP from the block diagram and click on **Make External** to have an external pin.

Figure 12: Making External Pin

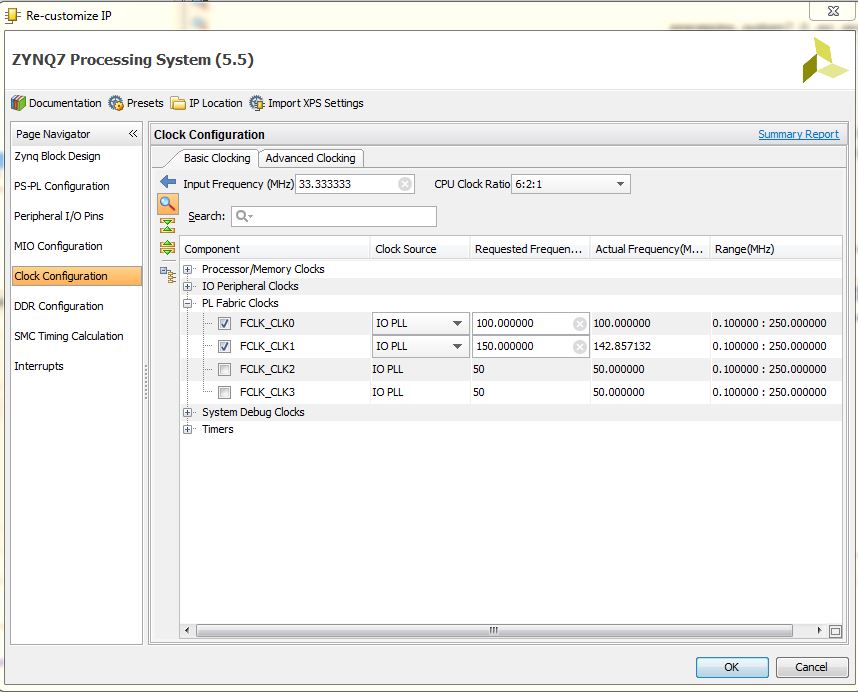
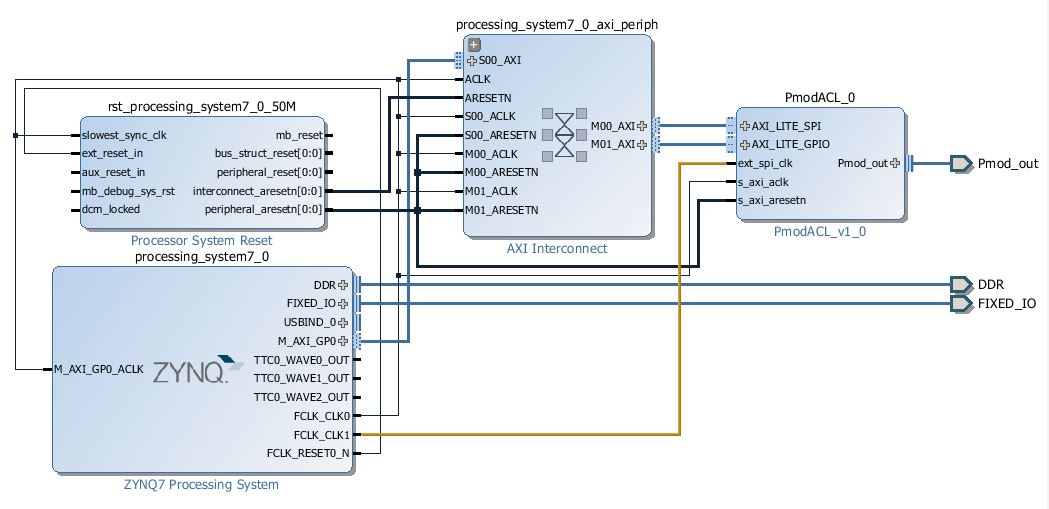
1. Double Click **ZYNQ7 Processing System > Clock Configuration > PL Fabric Clocks > Check FCLK\_CLK1**. Click **OK.**

Figure 13: Selecting FCLK\_CLK1.



1. Now, connect **FCLK\_CLK1** from **ZYNQ7 Processing System** to **ext\_spi\_clk** of **Pmod\_Acl\_0.**

Figure 14: Final Block Diagram

1. Select https://reference.digilentinc.com/_media/genesys2/validate.jpg **Validate Design**. This will check for design and connection errors.
2. Wrapper Creation: Right Click **design\_1.bd** , then select **Create HDL Wrapper** and click **OK.**

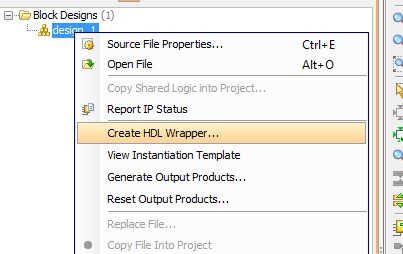


Figure 15 (a): Creation of HDL Wrapper

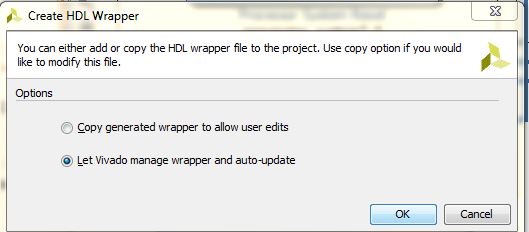


Figure 15 (b): Auto-updating of HDL Wrapper

1. Generate Bitstream: In the Program and Debug, select **Generate Bitstream.** And wait till the generation of bitstream.

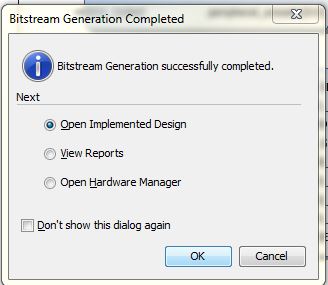
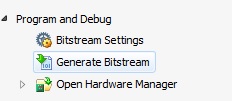


Figure 16: Bitstream Generation

# Export the hardware design to SDK

Once the bitstream has been generated, we can export our design to SDK where we can then write code for the PS. The PS is going to write data to our multiplier and read back the result.

1. In Vivado, from the File menu, select “**Export > Export hardware**”.

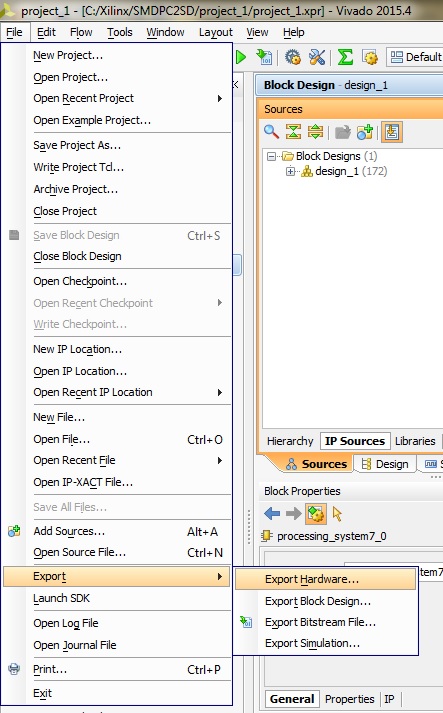


Figure 17: Export to Hardware

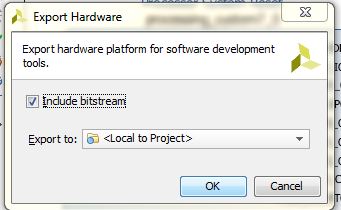
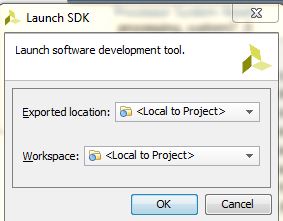
1. In the window that appears, tick “**Include bitstream**” and click “**OK**”.

Figure 18: Bitstream Inclusion

1. Again from the File menu, select “**Launch SDK**”. In the window that appears, use the following settings and click “**OK**”.



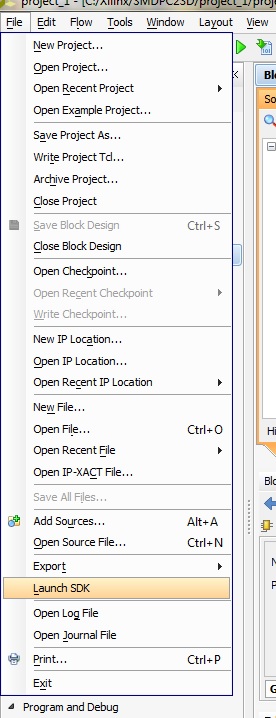
At this point, the SDK loads and a hardware platform specification will be created for our design. We should be able to see the hardware specification in the Project Explorer of SDK as shown in the image below.

Figure 19: Launch SDK

# Create a Software application

At this point, our SDK window should look somewhat like this:

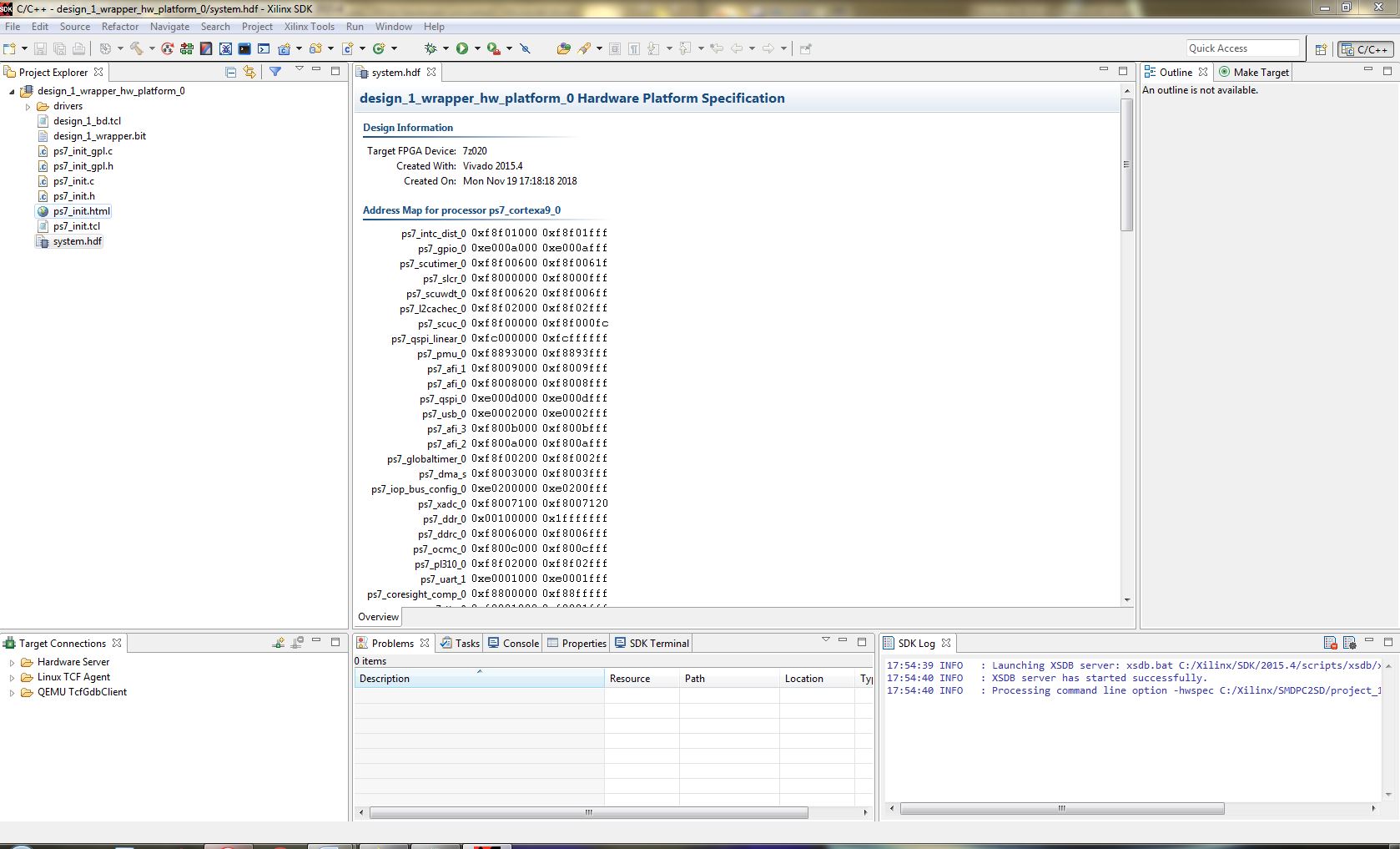


Figure 20: SDK Window

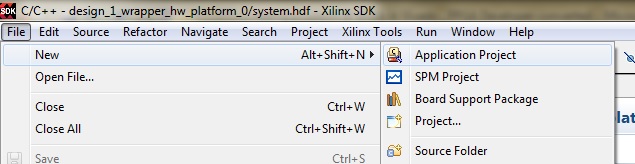
1. From the File menu, select **New** > **Application Project**.

Figure 21: Selection of Application Project

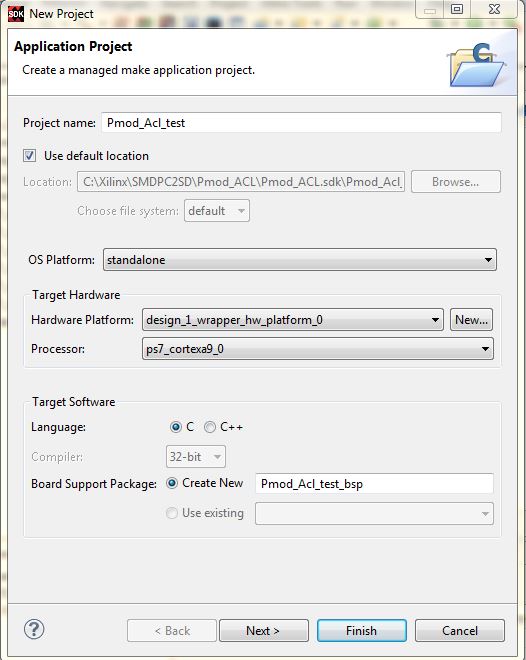
1. In the first page of the New Project wizard, choose a name for the application. We’ve chosen “**Pmod\_Acl\_test**”. Click “**Next**”.

Figure 22: Creation of Application Project

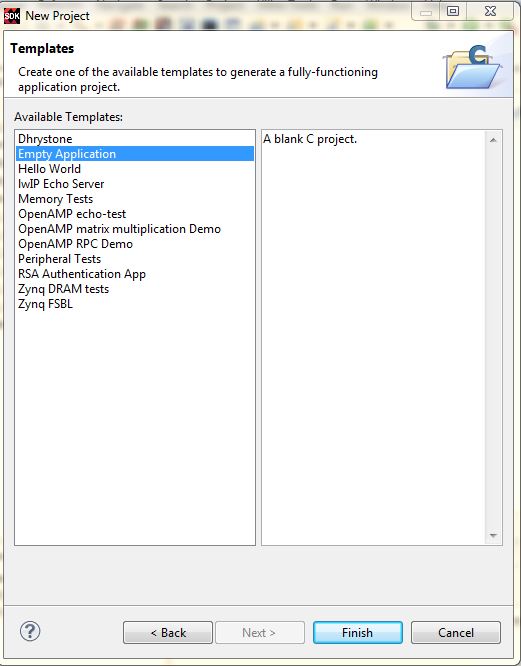
1. On the templates page, select the “**Empty Application**” template and click “**Finish**”.

Figure 23: Selection of a template

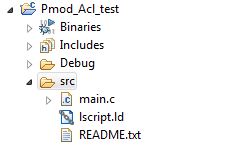
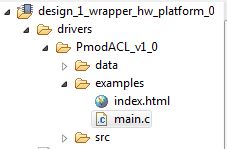
1. The SDK will generate a new application which we should find in the Project Explorer as in the image below. From Project Explorer Expand **design\_1\_wrapper\_hw\_platform\_0 > drivers > PmodACL\_v1\_0 > examples > main.c**. Select and copy (Ctrl + C) **main.c** and Paste (Ctrl + V) at Pmod\_Acl\_test > src.

Figure 24: Source folder of Pmod\_ACL\_test

# Test the design on the hardware

To test the design, we are using ZedBoard from Avnet.

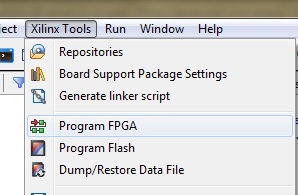
1. In the SDK, from the menu, select **Xilinx Tools** > **Program FPGA.**

Figure 25: Selecting Program FPGA

1. In the Program FPGA window, we select the hardware platform to program. We have only one hardware platform, so click “**Program**”.

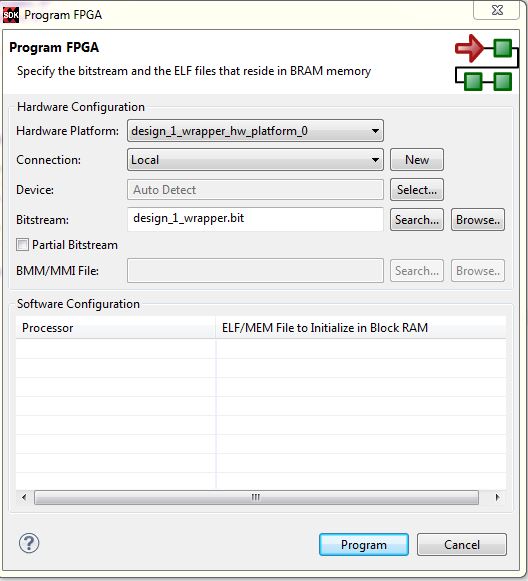
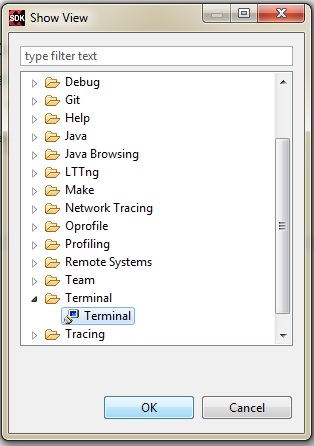
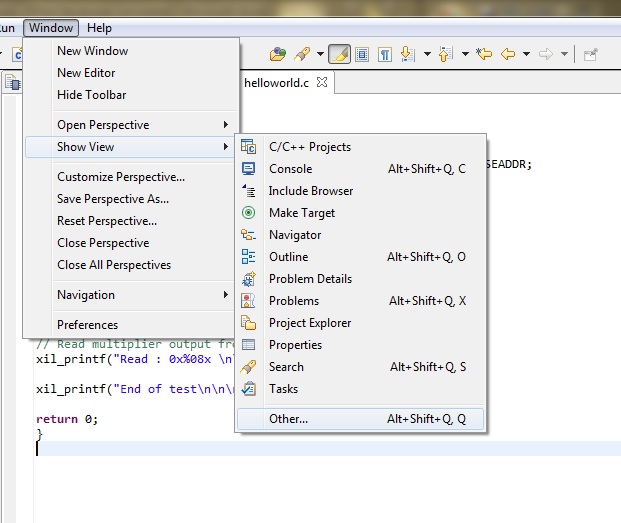
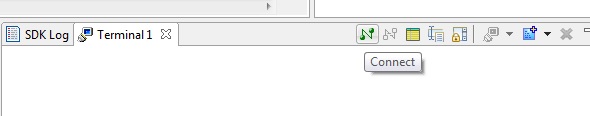


Figure 26: Programming of FPGA

1. Adding terminal: Add terminal to view the generated output. Select **Window > Show View > Other > Terminal > Terminal.**

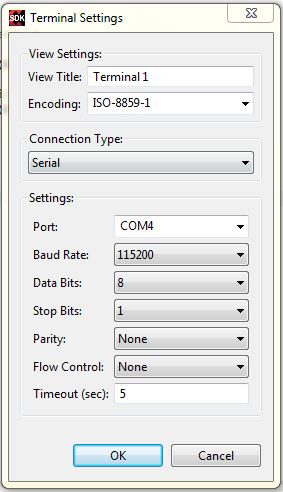
Figure 27: Addition of Terminal

1. Connecting Terminal

Figure 28: Connecting Terminal

Made the following changes in order to see the output in the terminal:

1. Connection Type: Serial
2. Port: COM4 (Nt.: It may be different with respect to PC, try selecting UART to USB Driver).
3. Baud Rate: 11520.



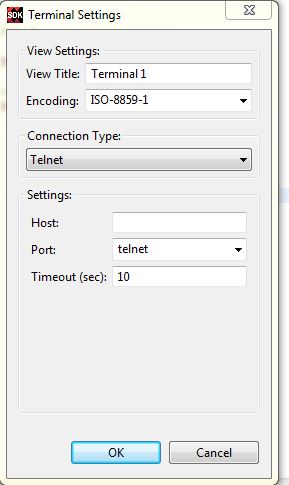


Figure 29: Configuration to Terminal

1. The bitstream will be loaded onto the Zynq and we are ready to load the software application. Select the “**multiplier\_test**” folder in the Project Explorer, and then from the menu, select **Run->Run**.
2. Click **Run As** https://reference.digilentinc.com/_media/genesys2/run.jpg button, select “**Launch on Hardware (System Debugger)**” and click “**OK**”.

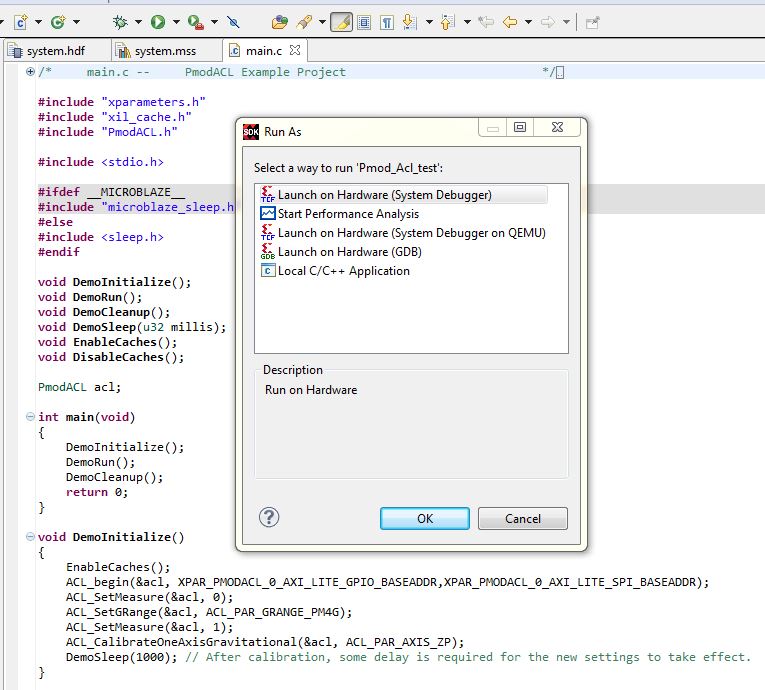


Figure 30: Launching Hardware

1. Output: Then again click **Run** to get the output in the terminal.

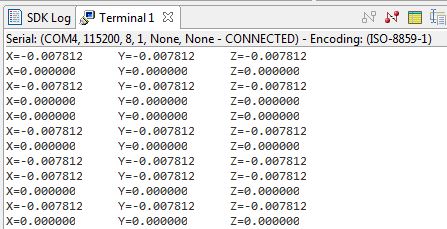


Figure 31: Output in the Terminal

1. We can also see the output in the Tera Term Software.
2. Open Tera Term.

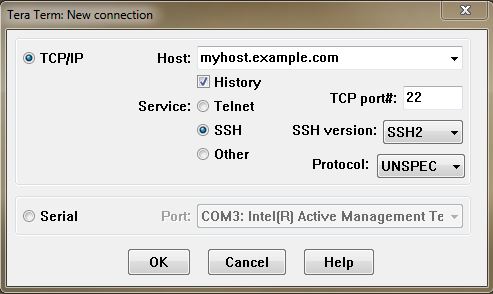


Figure 32: Tera Term

1. Select **Serial > COM4**

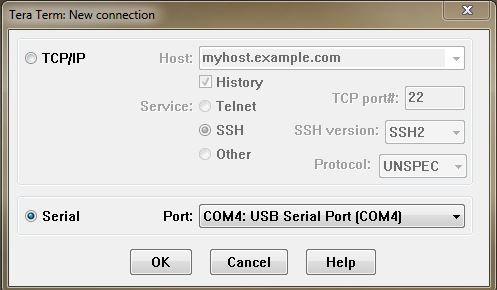


Figure 33: Selection of COM4: USB Serial Port

1. Click **Setup > Serial Port**. Change **Speed** to **115200** (Same as Baud Rate).

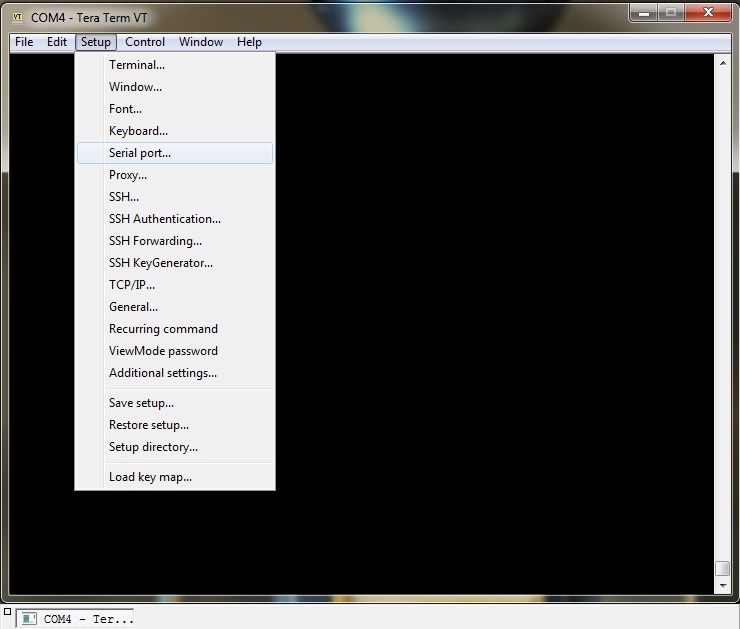
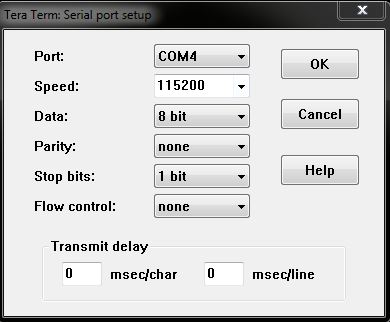


Figure 34: Setting up of Tera term

1. Output can be seen as the given figure

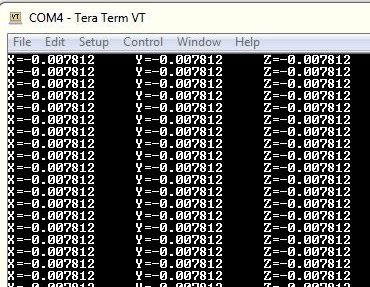


Figure 35: Output in the Tera Term

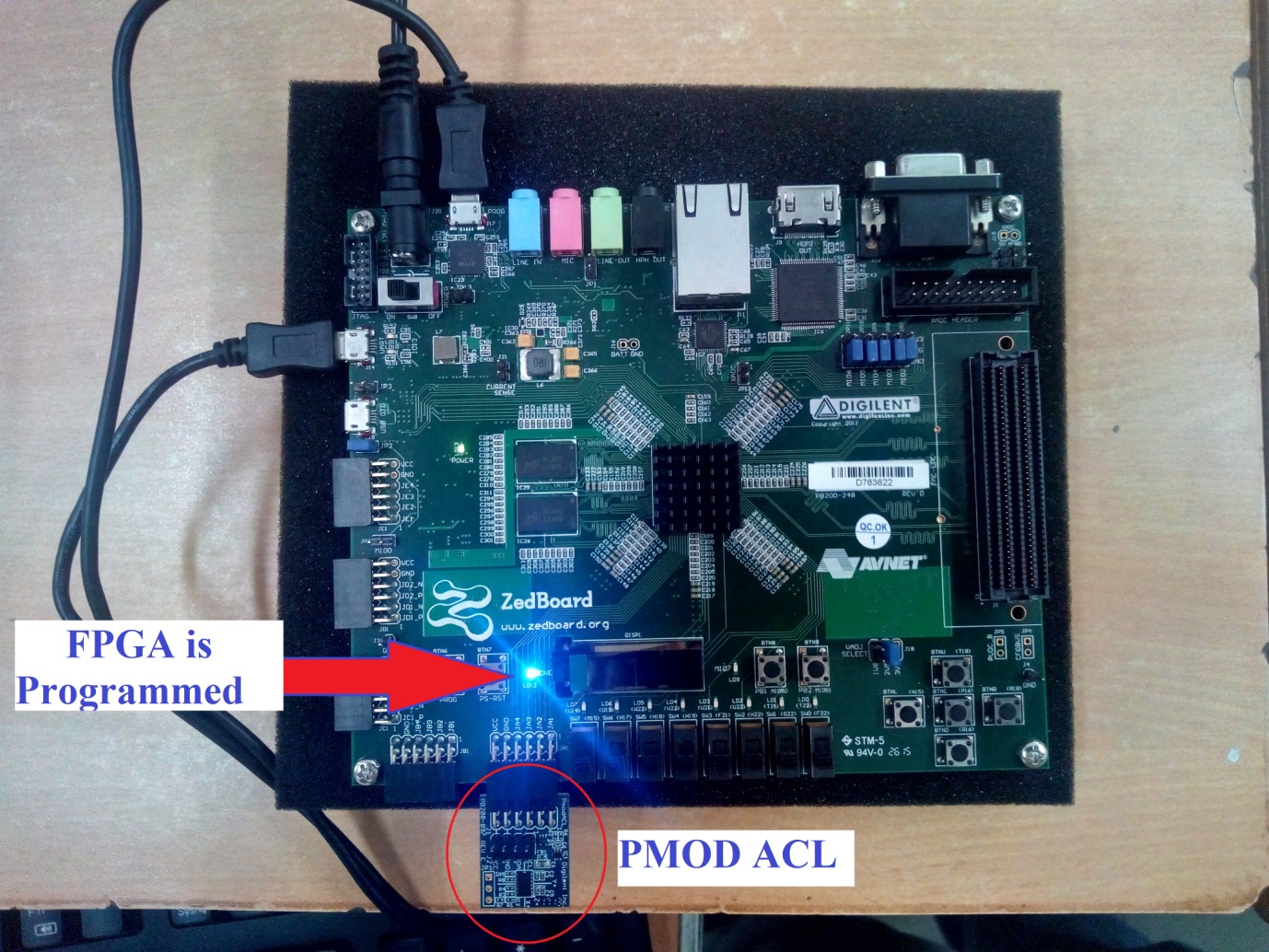


Figure 36: FPGA dumped with Program

# Creating whole model as IP

We can convert the whole design as a single IP and use the same in any other design.

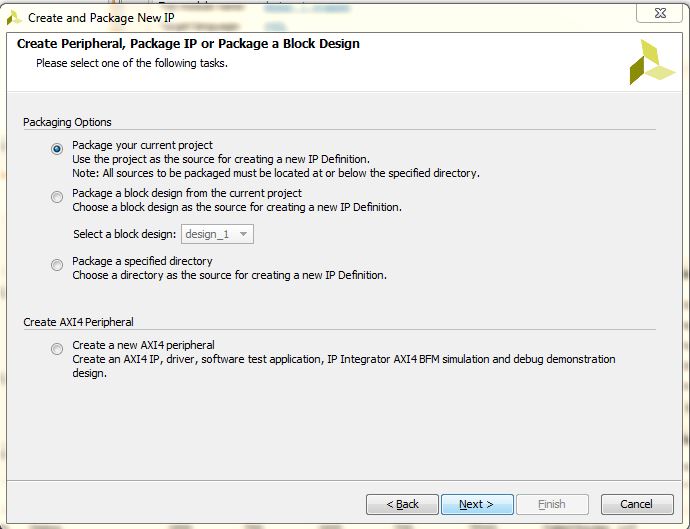
1. Select Tools **> Create and Package IP > Package your current project**. Click **Next**.

Figure 37: Packaging the Design

1. Click **Next**.
2. Click **Finish.**

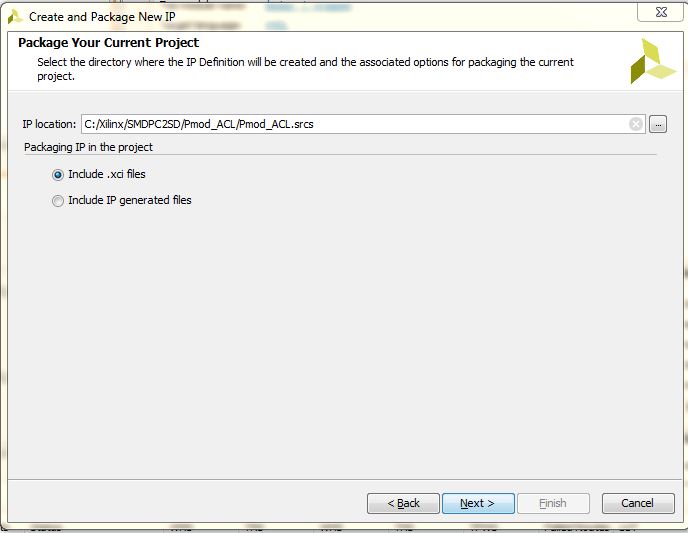


Figure 38: Creating IP from the design.

1. Then, follow the same processes as discussed earlier in the creation of a custom IP.